REMARKS

Applicant thanks the Examiner for acknowledging his claim to priority under 35 U.S.C. § 119, and receipt of a certified copy of the priority document.

Applicant thanks the Examiner for acknowledging acceptance of drawings filed on September 16, 2003.

Applicant corrected a typo in paragraph 0034 of the specification. The change is supported by Fig. 7 and the content of paragraph 0034. Nothing new has been introduced.

Claims 1-3 are all claims pending in the present application.

1. Claims 1-3 stand rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Applicant's Admitted Prior Art (AAPA) in view of Puziol et al. (USP 6,108,777). Applicant respectfully disagrees, because the Examiner's rejection is based upon improper hindsight.

The present application is related to a phase shifted binary transmission (PSBT) encoder. In the conventional PSBT encoders shown in Fig. 2, an exclusive or gate XOR with feedback is used. The feedback signal is delayed by one bit length. The delay is performed by a delay element ΔT or by a one-edge triggered D flip-flop FF1 clocked with a frequency corresponding to the bit rate. According to the present application, conventional PSBT encoders are either too inexact or too slow. In contrast, in the claimed invention, a transparent D flip-flop, instead of the one-edge triggered D flip-flop of the prior art encoder, is used to perform the delay.

Puziol is directed to reducing pipeline delays in high performance processors by anticipating taken branches through branch prediction. It has nothing to do with PSBT, or fast phase modulators.

In addition, although transparent D flip-flops are used in Puziol, they implement the logic, *e.g.*, constituting shift register of Fig. 3, for speculative execution in Figs. 5, 6 and 7. The transparent D flip-flops of Puziol are not used as delay elements.

Given the different goals of Puziol and the present application, there is no suggestion or motivation to combine the prior art encoder shown in Fig. 2 of the present application and Puziol. The only motivation for a skilled artisan to pick a transparent D flip-flop from Puziol and use it to replace the one-edge triggered D flip-flop shown in Fig. 2, as the Examiner has suggested, would be to reconstruct the claimed invention. However, the Examiner cannot rely on the present application for motivation; to do so would be impermissible hindsight. Accordingly, Applicant respectfully submits that claims 1-3 are allowable over the combination of AAPA and Puziol. Applicant respectfully requests reconsideration and withdrawal of the § 103(a) rejection of claims 1-3.

2. Claims 1-3 stand rejected under 35 U.S.C. 103(a) as being allegedly unpatentable over AAPA in view of Kojima et al. (U.S. Patent Application Publication US 2002/0196064). Applicant respectfully disagrees, because the Examiner's rejection is based upon improper hindsight.

Kojima directed towards to D-type latches used for sampling data with a clock and holding a sampled value, not for performing delay. According to Kojima, a perfectly balanced differential output latch would have the same time delay from a sampling clock edge to the generation of the inverting and non-inverting outputs. To avoid bad performance caused by timing jitter and skew, latches with well-balanced differential outputs are essential (Kojima, paragraphs 0002-0003).

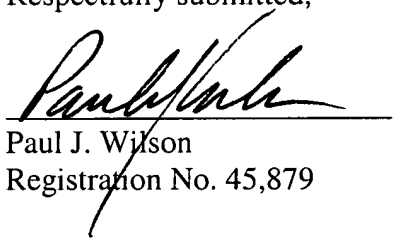
Kojima further discloses that hybrid-latch flip-flop (HLFF) have fast performance characteristics. However, claim 1 of the present application is directed towards fast phase modulators by using transparent D flip-flops, instead of providing flip-flops with fast performance. Further, the basis for replacing the one-edge triggered D flip-flop in the prior art encoder with the transparent D flip-flop is the property of the transparent D flip-flops, i.e., holding the output when the clock is 0 and propagating the changes on the input when the clock is 1. Whether the transparent D flip-flops have faster performance characteristics is not the primary concern. The substitution of the flip-flops of Kojima would not achieve the same functionality of the transparent D flop-flops of the present invention.

Thus, Kojima has nothing to do with the PSBT encoder. Given the different problems solved by the present application and Kojima, there is no suggestion or motivation for a skilled artisan to combine the references. Thus, the Examiner's combination of AAPA and Kojima is based upon is improper hindsight, and thus is improper.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



Paul J. Wilson
Registration No. 45,879

SUGHRUE MION, PLLC
Telephone: (202) 293-7060
Facsimile: (202) 293-7860

WASHINGTON OFFICE
23373
CUSTOMER NUMBER

Date: May 5, 2005